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3D 摄像模组规格书

3DCamera Module Approval Sheet

客户名称/ Customer	
客户型号/ Customer Project Name	
客户料号/ Customer Part No.	
机种型号/ JH Part No.	JH-B1011-01
确认时间/ Approval Date	

荆虹承认

JH Approval

PM 核准 PM Approved	研发审核 RD Checked	品质确认 QA Checked	制作 Prepared by

客户承认

Customer Approval

项目承认 PM Approval	品质承认 QA Approval	工程承认 PE Approval	采购承认 PUR Approval

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1 保证 Warranty

此规格摄像头，从荆虹出货之日起或客户收到产品后，至少一年内应符合下列正常条件下的储存和使用规格。

The products manufactured under these specifications shall be capable of meeting all characteristics within a minimum period of 1 year after shipment or the customer receives the products when stored and used as specified.

2 特征和规格 Features and General Specifications

Attribute	Parameter
Module Resolution	640*480@30fps
Module Size	28.3mm*52.7mm*5.52mm
IR Camera FOV	H:70°, V:54.7°, D:82.3°
Projector Power	Max 3W
VCSEL FOV	72° X58°
Wavelength	940nm
Power Supply	VCC_TOF: 3.3V (Peak current 1A); I/O: 1.8V (Peak current 200mA); Laser: 3.3V (Peak current 3.5A@1ns);
Power Consumption	Operating: 330mW@(30fps,4phase,Integ 1000uS)
Data Interface	2-Lane MIPI CSI-2, 800 Mbit/s
Control Interface	IIC, Slave address: 0111101B(0x3DH)
Support system	Linux (RK3326, RK3399, MR813, ...)
System frequency	24MHz, Accuracy ±500ppm
Modulation frequency	80MHz, 100MHz
Distance range	0.1-2.5m
Operating temperature	-20°C ~ 70°C
Laser Safety	LASER CLASS 1 (IEC 60825-1:2007/2014)

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2.1 关键部件规格 Key Component Specification

2.1.1 Chip specifications

Sensor	型号 Type	S5K33DXX (COB)
	光学尺寸 Optical size	1/3.2"
	有效像素 Active Array Size	640x480
	像素尺寸 Pixel Size	1.5umx1.5um
	输出方式 Output Data Format	MIPI
	运行温度范围 Operation temperature rang	-20°C ~ 70°C
	存储温度范围 Storage temperature rang	-40°C ~ 125°C

2.1.2 Lens specifications

Lens	型号 Type	
	F/NO	1.45±5%
	可视角 FOV(Field of View)	D82.3° H70° V54.7°
	结构 Construction	4P
	图像失真 TV-Distortion	<1.5%
	Max Image Circle	φ5.84mm
	EFL	3.16mm
	TTL	4.985mm
	螺纹参数 Barrel Thread	/

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2.1.3 Connector type

Connector	型号 Type	5055513420
	Pin 间距 Pin pitch	0.40 mm
	长度 Length Size	8.27 mm
	宽度 Width Size	2.1 mm
	高度 Height Size	0.68 mm
	工作温度范围 Operating temperature	-40°C to +85°C

3 模组规格及电气性能 Test Requirement and Electric characteristics

3.1 模组尺寸 Module Dimension

ROHS

Version	History	Originator	Date

SENSOR 主要参数		LENS 主要参数	
感光芯片 (Chip type)	S5K33DXX-C08-V3.2	焦距 (EFL)	3.16
像素 (Array size)	640X480 (VGA)	光圈 (F/NO)	1.45±5%
模拟电压 (AVDD)	2.8V	视场角 (View angle)	89.3° HFOV, V&A, 7°
数字电压 (DVDD)	1.05V	Chief Ray Angle	<30°
接口电压 (DOVDD)	1.8V	COMPOSITION	4P
芯片厚度 (Sensor thickness)	150um	TV-Distortion	<1.5%
芯片IC地址 (Sensor IIC)	/	胶深	0.29mm~INF (A1=0.7mm)
像素尺寸 (Pixel Size)	/	测试距离	0.7M
解析度	/	测试图	/

深圳荆虹科技有限公司			Title: B1011-01		
LEVEL TOLERANCE TYPE Devicr type DIM <3 ±0.03 ±0.03 ±0.1 ±0.15 >3~50 ±0.05 ±0.05 ±0.1 ±0.15 >50~100 ±0.05 ±0.08 ±0.15 ±0.2 >100 ±0.08% ±0.1% ±0.2 ±0.3% ANGLE ±0.5° ±0.5° ±0.8° ±3° Tilt angle 限位					
Size 尺寸		Unit	Scale	Sheet	
A4		mm	1:1	1 / 1	

NOTE: 1. "M" 号尺寸重点管控, CPK>1.33
 2. 公差标注参照 GB/T 1800.1-2009
 3. 80V: 1.8V, 35mA (VDDM, M=2.8V, 15mA)
 DVDD: 1.8V, 700mA (5mA, 1000P, 1000P)
 VDDIO: 1.8V, 100mA (VDDIO, 1000P, 1000P)
 4. Board: Active low
 5. 引脚 I/O: 1.45V (VDDIO, 1000P, 1000P)
 6. Board: Active low
 7. I/O 采用无源上拉电阻, 阻抗处理, WIP 阻抗 100±10%
 8. 封装: 贴片, 平均公差 ±10%, 200%
 9. 封装材料: 小于 0.1mm, 小于 0.1mm, 小于 0.1mm
 10. 10~100°C (25°C, 30°)
 11. 重量: 3.55g
 12. 平均公差: 75μm
 13. 1000P: 1.0P

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3.2 电气性能 Electric characteristics

- Absolute maximum rating**

Description	Symbol	Min.	Typ.	Max.	Unit
Digital absolute maximum	VDDD (max.)	-0.5	-	1.5	V
Analog absolute maximum	VDDA (max.)	-0.3	-	3.6	V
I/O absolute maximum	VDDIO (max.)	-0.3	-	3.6	V
PGD absolute maximum	VDDPG (max.)	-0.5	-	1.5	V
Digital input voltages, absolute max. ⁽¹⁾	VIP (max.)	-0.3	-	VDDIO + 0.3	V
VCAP analog voltages, absolute max. ⁽²⁾	VCAP	-0.3	-	4.2	V
Storage temperature	TSTR	-40	-	85	°C

- Operating Conditions**

Description	Symbol	Min.	Typ.	Max.	Unit
Digital power supply ⁽¹⁾	VDDD	0.95	1.05	1.15	V
Analog power supply ⁽²⁾	VDDA	2.7	2.8	2.9	V
I/O supply	VDDIO	1.7 (or 2.7)	1.8 (or 2.8)	1.9 (or 2.9)	V
PGD supply ⁽³⁾	VDDPG	0.95	1.05	1.15	V
Digital input voltages ⁽⁴⁾	VIP	0	-	VDDIO	V
VCAP analog voltage	VCAP	0	-	4.2	V
Test temperature (Ta) ⁽⁵⁾	TTEST	21	23	25	°C
Optimum operating temperature (Tj) ⁽⁶⁾	TOPT	0	-	60	°C
Normal operating temperature (Tj) ⁽⁷⁾	TOPR	-20	-	60	°C
Functional operating temperature (Tj) ⁽⁸⁾	TFUNC	-20	-	70	°C

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• **DC Characteristics**

(VDDA = 2.7 V to 2.9 V, VIP = 1.8 V ± 0.1 V or 2.8 V ± 0.1 V, T_j = -30 to +70°C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	0.7 × VIP	–	VIP + 0.3	V
	VIL	–	–0.3	–	0.3 × VIP	
Input leakage current	IIL	VIN = VIP or VSS	–10	–	10	μA
High-level output voltage	VOH	IOH = –100 μA	VDDIO – 0.2	–	–	V
Low-level output voltage	VOL	IOL = 100 μA	–	–	0.2	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	–10	–	10	μA
Input capacitance	CIN	–	–	–	5	pF
Supply current	IHWSBA ⁽¹⁾	Hardware standby mode, analog	–	TBD	TBD	μA
	IHWSBD ⁽¹⁾	Hardware standby mode, digital	–	TBD	TBD	
	ISTRMA ⁽²⁾	Streaming mode, analog, 4-tap @ 60 fps	–	TBD	TBD	mA
	ISTRMD ⁽²⁾	Streaming mode, digital, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMIO ⁽²⁾	Streaming mode, I/O, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMP ⁽²⁾	Streaming mode, PGD, 4-tap @ 60 fps	–	TBD	TBD	

• **AC Characteristics**

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency ⁽¹⁾	fXCLK	–	6	–	64	MHz
External clock duty cycle ⁽¹⁾	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	--	–	500	μs

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- I2C Standard Mode Timing Specifications**

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for start condition	T ₁	4.0	–	μs
Setup time for stop condition	T ₂	4.0	–	
Data setup time	T ₃	250	–	ns
Data hold time	T ₄	0	3.45	μs
High period of the SCL clock	T ₅	4.0	–	
Low period of the SCL clock	T ₆	4.7	–	
Bus free time between stop and start conditions	T ₇	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

- I2C Fast Mode Timing Specifications**

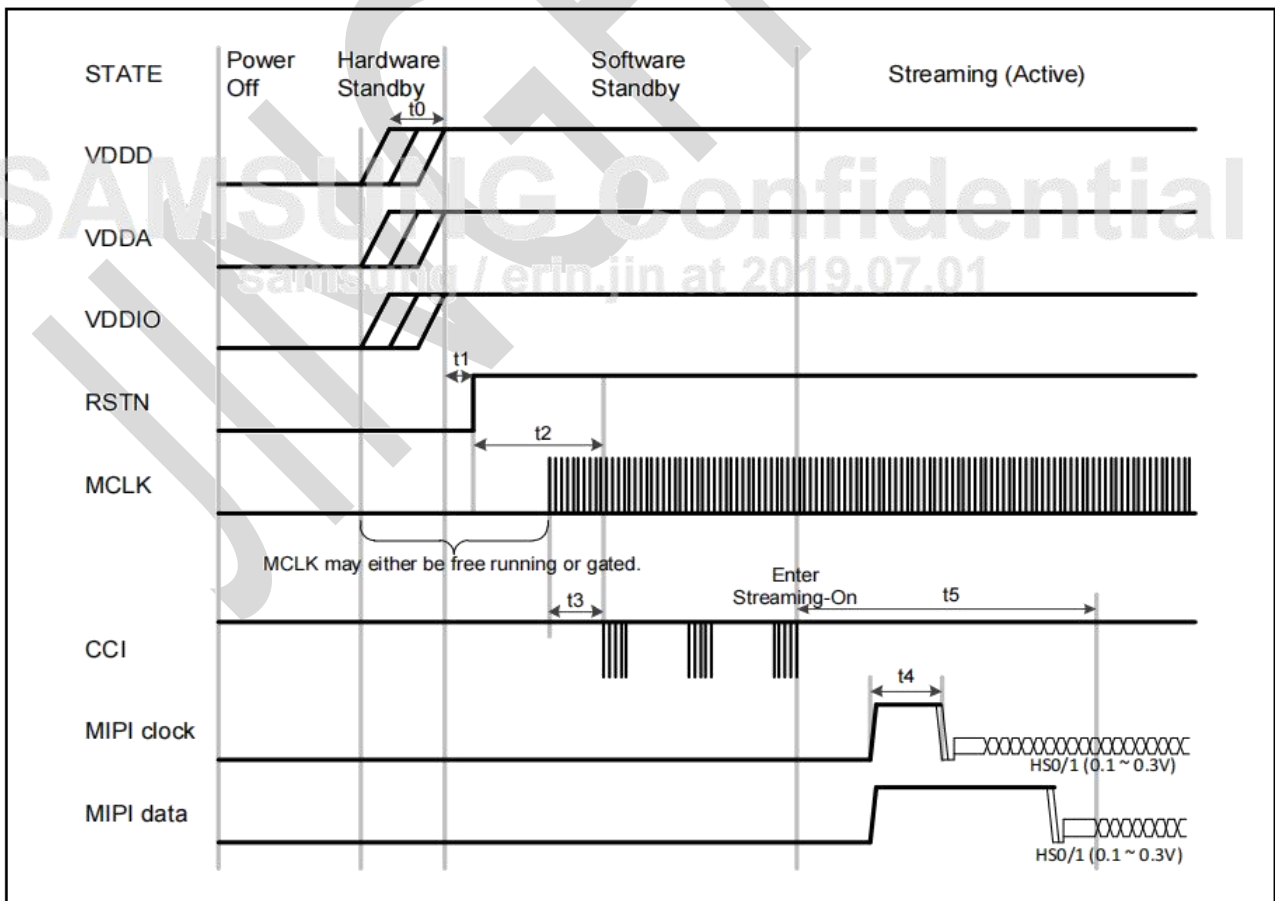
Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T ₁	0.6	–	μs
Setup time for stop condition	T ₂	0.6	–	
Data setup time, external clock (MCLK) above 12.8 MHz	T ₃	0.1	–	μs
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T ₄	0	0.9	μs
High period of the SCL clock	T ₅	0.6	–	
Low period of the SCL clock	T ₆	1.3	–	
Bus free time between stop and start conditions	T ₇	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

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• **I2C Fast Mode Plus(FM+) Timing Specifications**

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	1	MHz
Hold time for start condition	T ₁	0.26	–	μs
Setup time for stop condition	T ₂	0.26	–	
Data setup time, external clock (MCLK) above 24 MHz	T ₃	0.05	–	μs
Data setup time, external clock (MCLK) between 12.8 and 24 MHz		0.1	–	
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T ₄	0	–	μs
High period of the SCL clock	T ₅	0.26	–	
Low period of the SCL clock	T ₆	0.5	–	
Bus free time between stop and start conditions	T ₇	0.5	–	ns
Rise time for both SDA and SCL signals	–	–	120	
Fall time for both SDA and SCL signals	–	–	120	
Capacitive load for each bus line	CB	–	550	pF

• **上电顺序 Power-UP Sequence**



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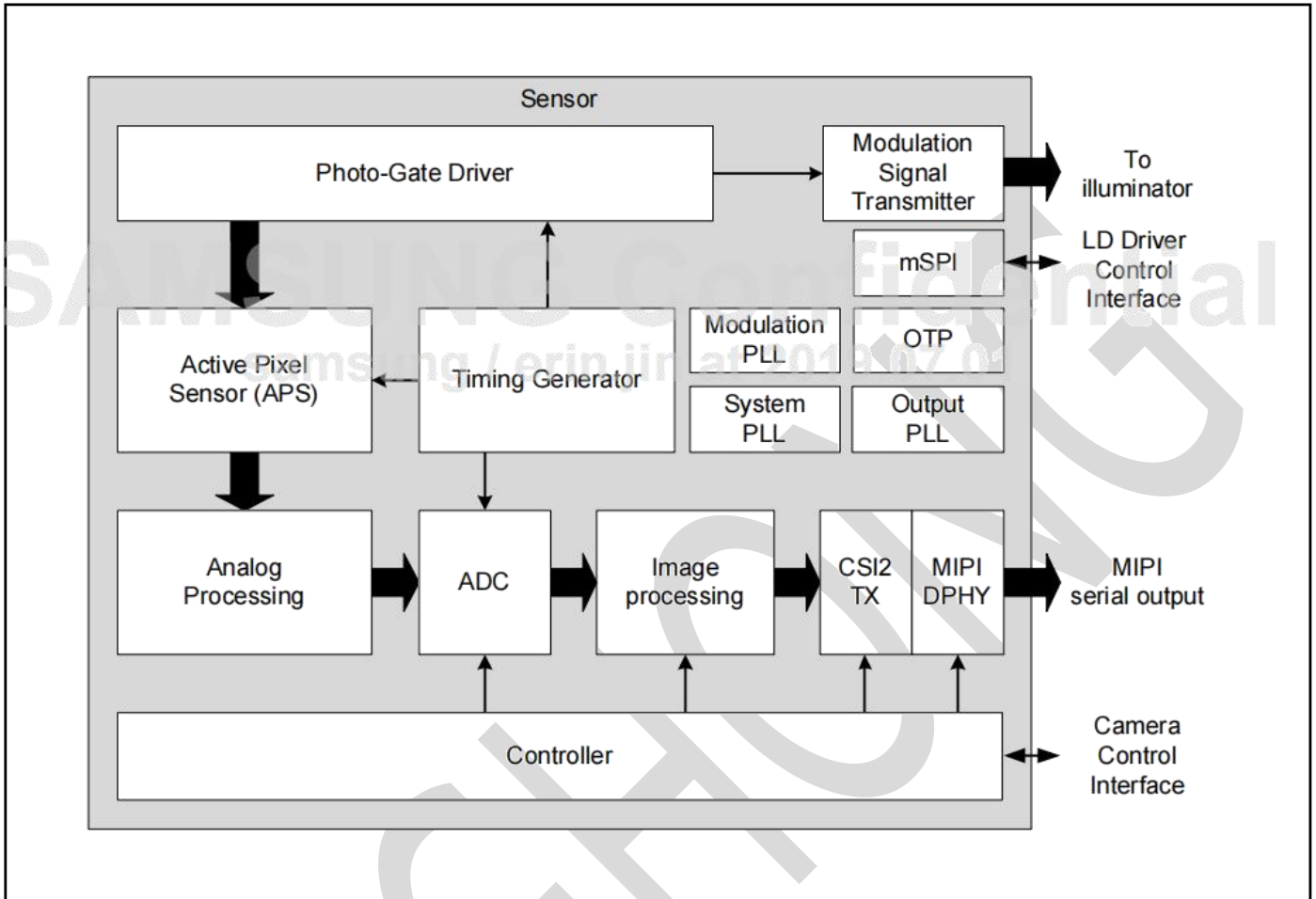
- Power-Up Sequence Timing Constraints**

Constant	Label	Min.	Max.	Unit
VDDA/VDDD/VDDIO rising time	t0	VDDA/VDDD/VDDIO may rise in any order. The rising separation can vary from 0 ns to indefinite.		ns
VDDD rising to RSTN (XSHUTDOWN) rising	t1	0.0	–	ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t2	10	–	μs
Minimum no. of MCLK (EXTCLK) cycles prior to the first CCI transaction	t3	23,000	–	MCLK cycles
PLL startup/lock time	t4	–	1	ms
DPHY initialization period (TINIT)	t5	0.1	–	ms
Entering streaming mode - The first frame start sequence	t6	+ the delay according to the coarse integration time value		-

备注：详细电气性能信息，请参考芯片规格书。

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3.3 系统框图 Block Diagram



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3.4 Pin 定义 Pin Description

No.	名称 Signal name	I/O	描述 Description
1	VCC_3V3_TOP	Power	3.3V
2	VCSEL_3.3V	Power	3.3V
3	VCC_3V3_TOP	Power	3.3V
4	VCSEL_3.3V	Power	3.3V
5	GND	Ground	System reference ground
6	VCSEL_3.3V	Power	3.3V
7	GND	Ground	System reference ground
8	VCSEL_3.3V	Power	3.3V
9	IOVDD_TOF	Power	Power for I/O circuit; 1.8V, I _{max} =200 mA
10	GND	Ground	System reference ground
11	NC	-	No connection(terminal NC)
12	NC	-	No connection(terminal NC)
13	NC	-	No connection(terminal NC)
14	XVS	O	Vertical sync .output
15	MCLK	Input	Main clock input
16	NC	-	No connection
17	GND	Ground	System reference ground
18	GND	Ground	System reference ground
19	CSI_DO_P	Output	MIPI CSI-2 Data Output 0 - positive
20	I2C_SCL	Input	SPI mode:Serial clock input,IIC mode:IIC input clock
21	CSI_DO_N	Output	MIPI CSI-2 Data Output 0 - negative
22	I2C_SDA	O	SPI mode:Serial data output,IIC mode:no connection
23	GND	Ground	System reference ground
24	GND	Ground	System reference ground
25	CSI_CL_P	Output	MIPI CSI-2 Clock Output - positive
26	RESET	Input	Master reset,active low (XSHUTDOWN)
27	CSI_CL_N	Output	MIPI CSI-2 Clock Output - negative
28	NC	-	No connection
29	GND	Ground	System reference ground
30	NC	-	No connection
31	CSI_D1_P	Output	MIPI CSI-2 Data Output 1 - positive
32	NC	-	No connection
33	CSI_D1_N	Output	MIPI CSI-2 Data Output 1 - negative
34	NC	-	No connection